IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Previously Presented): A non-volatile semiconductor memory comprising:

a memory cell array having a plurality of non-volatile memory cells;

a decode circuit configured to decode address data as input thereto to select a memory cell of said memory cell array; and

a data sense circuit configured to sense and amplify data of the selected memory cell of said memory cell array, wherein

said memory cell array includes an initial setup data region with initial setup data programmed thereinto, said initial setup data being for determination of memory operating conditions.

Claim 2 (Previously Presented): The non-volatile semiconductor memory according to claim 1, wherein

said memory cell array has a redundant cell array adapted to be used for replacement of a defective memory cell, said initial setup data including defect address data, and further comprising:

a defect address register configured to store therein said defect address data as read out of said initial setup data region and transferred therefrom and to perform replacement control of said defective memory cell.

Claim 3 (Previously Presented): The non-volatile semiconductor memory according to claim 2, further comprising:

a data latch circuit associated with said decode circuit configured to set a row decoder corresponding to a defective row in an inactive state based on said defect address data as read out of said initial setup data region.

Claim 4 (Previously Presented): The non-volatile semiconductor memory according to claim 2, further comprising:

a data latch circuit associated with said data sense circuit configured to set a sense amplifier corresponding to a defective column in an inactive state based on said defect address data as read out of said initial setup data region.

Claim 5 (Previously Presented): The non-volatile semiconductor memory according to claim 1, wherein

said nonvolatile memory cells are electrically rewritable, said initial setup data including voltage data for designation of a voltage used for data writing and erasure of said memory cell array, and further comprising:

a voltage setup register configured to store therein said voltage data as read out of said initial setup data region for execution of voltage control during data writing and erasing.

Claim 6 (Previously Presented): The non-volatile semiconductor memory according to claim 1, wherein

said initial setup data includes chip information data, and further comprising:

a chip information register configured to store therein said chip information data as read out of said initial setup data region.

Claim 7 (Previously Presented): A non-volatile semiconductor memory comprising:

a memory cell array having a plurality of non-volatile memory cells, said memory cell array having an initial setup data region with initial setup data programmed thereinto, said initial setup data being for determination of memory operating conditions;

a decode circuit configured to decode input address data to select a memory cell of said memory cell array;

a data sense circuit configured to sense and amplify data of the selected memory cell of said memory cell array;

an operating condition setting circuit configured to store therein said initial setup data as read out of said initial setup data region and transferred therefrom and to control memory operating conditions; and

a control circuit configured to control transfer of said initial setup data toward said operating condition setting circuit.

Claim 8 (Original): The non-volatile semiconductor memory according to claim 7, wherein

said memory cell array has a redundant cell array used for replacement of a defective memory cell, said initial setup data including defect address data, and wherein said operating condition setting circuit has a defect address register configured to store therein said defect

address data read out of said initial setup data region and sent therefrom and for performing control of replacement of said defective memory cell.

Claim 9 (Original): The non-volatile semiconductor memory according to claim 7, further comprising;

a data latch circuit associated with said decode circuit configured to set a row decoder corresponding to a defective row in an inactive state based on said defect address data as read out of said initial setup data region.

Claim 10 (Previously Presented): The non-volatile semiconductor memory according to claim 8, further comprising:

a data latch circuit associated with said data sense circuit configured to set a sense amplifier corresponding to a defective column in an inactive state based on said defect address data as read from said initial setup data region.

Claim 11 (Original): The non-volatile semiconductor memory according to claim 8, wherein

said non-volatile memory cells are electrically rewritable, said initial setup data including voltage data for designation of a voltage used for data writing and erasure of said memory cell array, and wherein said operating condition setting circuit has a voltage setup register configured to store therein said voltage data as read and sent from said initial setup data region and to perform voltage control during data writing and erasing.

Claim 12 (Original): The non-volatile semiconductor memory according to claim 8, wherein

said initial setup data includes chip information data, and wherein said operating condition setting circuit has a chip information register configured to store therein said chip information data as read and sent from said initial setup data region.

Claim 13 (Original): The non-volatile semiconductor memory according to claim 7, wherein

said initial setup data region has a first initial setup data block with initial setup data being programmed thereinto and a second initial setup data block with initial setup data identical to the data of said first initial setup data block being programmed thereinto.

Claim 14 (Previously Presented): The non-volatile semiconductor memory according to claim 13, wherein

in case said first initial setup data block is normal, said initial setup data is programmed into said first initial setup data block whereas when said first initial setup data block is defective, said initial setup data is programmed into said second initial setup data block.

Claim 15 (Previously Presented): The non-volatile semiconductor memory according to claim 7, wherein

said initial setup data is comprised of at least one set of data satisfying a complementary relationship therebetween.

Claim 16 (Previously Presented): The non-volatile semiconductor memory according to claim 8, wherein

said initial setup data region comprises evennumbered pages defined as even-numbered bitlines range for allowing defective column address data included in said defect address data to be programmed thereinto, and odd-numbered pages defined as odd-numbered bitlines range for allowing defective row address data to be programmed thereinto.

Claim 17 (Previously Presented): The non-volatile semiconductor memory according to claim 16, wherein

said even-numbered pages permit N (where "N" is a positive integer) sets of defective column address data satisfying complementary relations respectively to be programmed thereinto, and wherein said odd-numbered pages permit M (where "M" is a positive integer less than N) sets of defective row address data satisfying complementary relations respectively to be programmed thereinto.

Claim 18 (Original): The non-volatile semiconductor memory according to claim 7, wherein

said control circuit becomes automatically operative upon detection of power activation for controlling reading of said initial setup data and also transferring such read data toward said operating condition setter circuit.

Claim 19 (Original): The non-volatile semiconductor memory according to claim 7, wherein

said control circuit is responsive to input of a command for controlling reading of said initial setup data and also transferring such read data toward said operating condition setting circuit.

Claim 20 (Original): The non-volatile semiconductor memory according to claim 7, wherein

said memory cell array comprises a NAND cell unit with a series connection of a plurality of electrically rewritable non-volatile memory cells.

Claim 21 (Original): The non-volatile semiconductor memory according to claim 20, wherein

said initial setup data region comprises at least one cell block including a plurality of NAND cell units, the cell block being used as a unit for data erasure.

Claim 22 (Previously Presented): The non-volatile semiconductor memory according to claim 20, wherein

said initial setup data is programmed with an all "0" state in a single NAND cell unit and all "1" state in a single NAND cell unit, the all "0" state and all "1" state serving as one bit data, respectively.

Claim 23 (Currently Amended): A non-volatile semiconductor memory comprising:

a memory cell array with non-volatile memory cells disposed therein, having an initial setup data region with a first and a second data block, said first data block permitting initial setup data for determination of memory operating conditions to be programmed thereinto, said second data block allowing data identical to that of the first data block to be programmed thereinto;

a decode circuit configured to decode input address data to select a memory cell of said memory cell array; and

a data sense circuit configured to sense and amplify the selected memory cell of said memory cell array.

Claim 24 (Currently Amended): The non-volatile semiconductor memory according to claim 23, wherein

in case said first data block is normal, said initial setup data is programmed into said first data block whereas when said first data block is defective, said ~~and~~ initial setup data is programmed into said second data block.

Claim 25 (Previously Presented): The non-volatile semiconductor memory according to claim 23, wherein

said memory cell array has a redundant cell array adapted to be used for replacement of a defective memory cell, said initial setup data including defect address data, and further comprising:

a defect address register configured to store therein said defect address data as read out of said initial setup data region and transferred therefrom and for performing replacement control of said defective memory cell.

Claim 26 (Previously Presented): The non-volatile semiconductor memory according to claim 25, further comprising:

a data latch circuit associated with said decode circuit for setting a row decoder corresponding to a defective row in an inactive state based on the defect address data as read out of said initial setup data region.

Claim 27 (Previously Presented): The non-volatile semiconductor memory according to claim 25, further comprising:

a data latch circuit associated with said data sense circuit configured to set a sense amplifier corresponding to a defective column in an inactive state based on said defect address data as read from said initial setup data region.

Claim 28 (Previously Presented): The non-volatile semiconductor memory according to claim 25, wherein

said non-volatile memory cells are electrically rewritable, said initial setup data including voltage data for designation of a voltage used for data writing and erasure of said memory cell array, and further comprising:

a voltage setup register configured to store therein said voltage data as read and sent from said initial setup data region for execution of voltage control during data writing and erasing.

Claim 29 (Previously Presented): The non-volatile semiconductor memory according to claim 25, wherein

said initial setup data includes chip information data, and further comprising:

a chip information register configured to store therein said chip information data as read and sent from said initial setup data region.

Claim 30 (Previously Presented): The non-volatile semiconductor memory according to claim 23, wherein

said initial setup data is comprised of at least one set of data satisfying a complementary relationship there between.

Claim 31 (Previously Presented): The non-volatile semiconductor memory according to claim 25, wherein

said initial setup data region comprises an even numbered pages defined as even-numbered bitlines range for allowing defective column address data included in said defect address data to be programmed thereinto and odd-numbered pages defined as odd-numbered bitlines range for letting defective row address be programmed thereinto.

Claim 32 (Previously Presented): The non-volatile semiconductor memory according to claim 31, wherein

said even-numbered pages permit N (where "N" is a positive integer) sets of defective column address data satisfying complementary relations respectively to be programmed thereinto, and wherein said odd-numbered pages permit M (where "M" is a positive integer less than N) sets of defective row address data satisfying complementary relations respectively to be programmed thereinto.

Claim 33 (Original): The non-volatile semiconductor memory according to claim 23, wherein

said memory cell array comprises a NAND cell unit with a series connection of a plurality of electrically rewritable non-volatile memory cells.

Claim 34 (Original): The non-volatile semiconductor memory according to claim 33, wherein

said initial setup data region comprises at least one cell block including a plurality of NAND cell units, said cell block being used as a unit for data erasure.

Claim 35 (Previously Presented): The non-volatile semiconductor memory according to claim 33, wherein

said initial setup data is programmed with an all "0" state in a single NAND cell unit and all "1" state in a single NAND cell unit, the all "0" state and all "1" state serving as 1-bit data respectively.